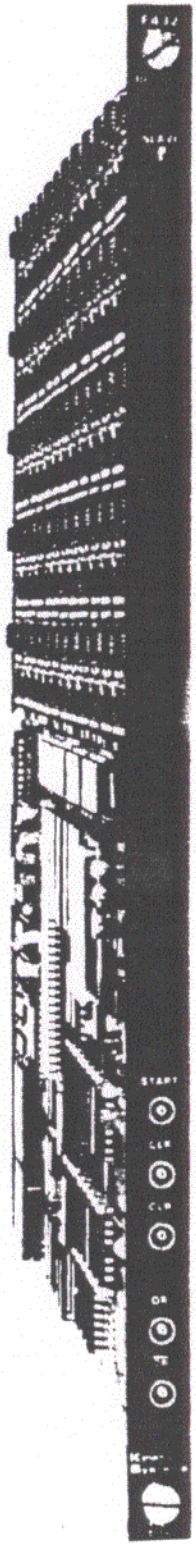
FASTBUS F432

64-channel Time-to-Digital Converter

(Rev. Oct. 90)



FEATURES

- Standard single-width FASTBUS module
- 64 independent channels with common Start input, front-panel NIM Start input, or ECL level Start input accessible from auxiliary backplane
- All channel Stop inputs received as differential ECL pairs accessible from the FASTBUS auxiliary backplane
- 25 picosecond resolution / approximately 100 nanosecond full-scale range
- Less than 2 LSB integral and differential nonlinearity over the entire full-scale range
- Unique zero-surpressed block transfer mode
- Automated calibration mode for pedestal determinations
- Fast clear time (one microsecond)
- Addressable through logical or geographical modes
- Addressable through FASTBUS Broadcasts including sparse data, T pin, and Class N scans
- On-board Hit register indicates channels with valid data
- Optional user input for control of Hit register clock

GENERAL DESCRIPTION

The F432 Time-to-Digital Converter (TDC) is a very high-resolution device with the requisite linearity to precisely resolve time intervals within ±50 picosecond steps. This is the first commercially available FASTBUS device designed to meet this criterion.

Sixty-four TDC channels are packaged on a standard single-width FASTBUS module using 64 single-channel daughter boards. This allows convenient replacement for in-the-field serviceability. The device differentially measures the time interval between a Start input pulse and each channel's Stop input pulse. The design utilizes a factory calibrated digital compensation for offset and gain errors on a per channel basis. This results in a 12-bit range of corrected values, allowing a full-scale range of approximately 100 nanoseconds with 25 picosecond/LSB. This correction technique ensures less than ±2 LSB integral and differential nonlinearity for each channel.

The time from onset of the Start pulse to the completion of digital conversion for all channels is guaranteed to be less than 300 microseconds. A negligible clear time of 100 microseconds allows separate events to be recorded in rapid succession. When the conversions are completed and data is available for transfer over FASTBUS, an SR interrupt can be issued by the TDC when enabled by Bit 4 of CSR0. The host may then perform a sparse data scan operation (Case 3) or TP scan (Case 5) on a particular crate to determine which TDC modules have valid information to be transferred. Having accessed a TDC containing valid data, the host simply reads any or all channels with either a block transfer or separate single-word data cycles. Alternatively, the host can interrogate a Hit register whose bit locations, when tested, indicate which channels have valid data. The latching of the "Hit" status of the channels is defaulted to occur at the full-scale time of 100 nanoseconds after a Start input pulse. However, a front-panel input available to the user freezes the Hit register anytime before this default.

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GENERAL DESCRIPTION *(continued)*

By far the fastest and most ingenious method for reading valid data from the F432 over FASTBUS is the special zero-suppressed block mode. When enabled by Bit 23 of CSRO, a block or pipelined Read causes only those channels whose Stop input pulses occurred before the 100 nanoseconds full-scale time to be sequentially transferred. Intervening channels which overflowed or were never "Hit" will be automatically skipped. After the last valid channel is read, the F432 responds with SS = 2 (End-of-Block status) informing the current FASTBUS Master that the module has completely transferred all valid channel information. This unique collection technique saves substantial amounts of system memory that is otherwise wasted storing invalid data. At the same time, computer time is saved from transferring invalid channel data or searching out and separately addressing valid channels using the slower FASTBUS single-word transfers.

Host software overhead during data acquisition time is further reduced by first performing a calibration run which creates and stores a pedestal value for each channel in the F432 before data collection begins. When real data is collected, these pedestals are automatically subtracted by the hardware within the TDC module. In this way, corrected data is read directly by the host.

All 64 Stop inputs are connected to the TDC through a half-height Model F155-A21 board inserted in the rear auxiliary backplane slot opposite the TDC. The cable connectors on this board accept mass-terminated, shielded twisted pairs driven as differential ECL signals. A front-panel, single-pin LEMO connector serves as the input for NIM level Start pulses. Alternatively, an ECL level, differential pair connected to the auxiliary backplane may be used as the Start trigger.

ORDERING INFORMATION

Model F432-A01	—	High-resolution Time-to-Digital Converter
	—	25 picosecond resolution / ±2 LSB differential nonlinearity
Model F432-A02	—	High-resolution Time-to-Digital Converter
	—	50 picosecond resolution / ±2 LSB differential nonlinearity
Model F432-A03	—	High-resolution Time-to-Digital Converter
	—	100 picosecond resolution / ±2 LSB differential nonlinearity
Model F432-A04	—	High-resolution Time-to-Digital Converter
	—	150 picosecond resolution / ±2 LSB differential nonlinearity
Model F432-A20	—	Medium-resolution Time-to-Digital Converter
	—	1 nanosecond resolution / ±1 LSB differential nonlinearity
Accessories	—	Model F900-A01 — Segment Interconnect Model F901-A01 Segment/Cluster Interconnect with Route Table RAM Model F914-A01 — Q-bus® Processor Interface Model F930-A01 — Block Mover II Model F820-A01 — Scanner Processor Model F155-A21 — TDC Auxiliary Cable Card

G119 INPUT CARD $230

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